ECE310 Formal Report

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Summary

In ECE310 Labs 1 through 5 we built a communication system that transmitted a Pseudorandom generated sequence from a transmitter through an infrared LED that was then detected by a receiver via a phototransistor. The bit rate of the system was 100 bits per second. The transmission system can be broken down into varying subsystems such as: Pseudorandom data generator, carrier frequency generator, modulator, and an Infrared LED transmitter. Using a PIC 16F690 microcontroller, we were able to program a PSG that feeds into the modulator. The carrier frequency generator produces a square-wave carrier signal at 40kHz with a 50% duty cycle using an LM555 timer. The carrier is modulated with the PSG signal to produce a 1 when switched on and a 0 when switched off. The modulator can be constructed by a simple AND gate that drives a transistor. The output of the modulator can then be passed into an LED transmitter.

The receiver system can be dissected into the following subsystems: Transimpedance amplifier, Bandpass filter, envelope detector, comparator, receiver clock generator, and a flip flop. The trans-impedance amplifier converts the current from the phototransistor to a usable voltage. It is then fed into a bandpass filter to filter out noise from the environment and only have the message received. After the filter, the envelope detector demodulates the signal to convert it back to the original message that was generated before modulation. Next, the comparator decides if the message is a “1” or a “0”. In parallel a receiver clock is generated so that the transmitter’s clock does not have to supply the receiver’s clock. The message and transmitter’s clock are then fed to a flip flop which outputs the original message that was created from the PSG.

Introduction

The objective of this report is to provide a thorough overview of the subsystems of a communication transmitter and receiver. The functionality of the communication system design will be expanded upon in the System Overview. A more detailed schematic of the subsystems will be provided in the Circuit Documentation. The operation of the subsystems can be verified through scope captures at each output and will be entailed in the Measurements section of the report. To summarize and assess the quality of the communication system, a thorough analysis of the result will be expanded upon in the Discussion section.

System Overview

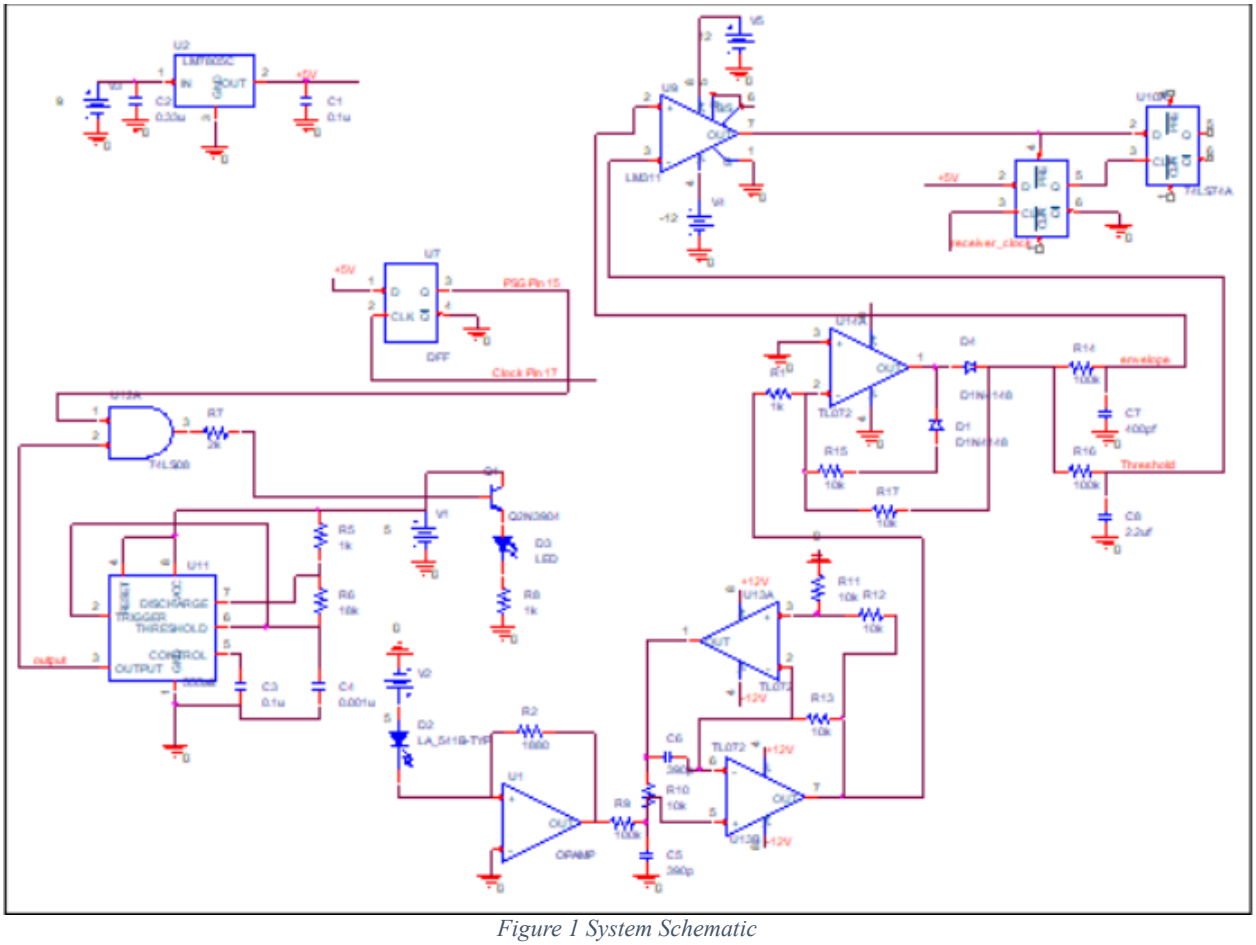

Figure 1 System Schematic

The PSG is the start of the system, and its purpose is to create a random message that will be transmitted. The PSG can be modeled by 20 flip flops and a few XOR gates as shown in Figure 2. It will create a message that appears random in a short period but this signal does repeat every 655 seconds.

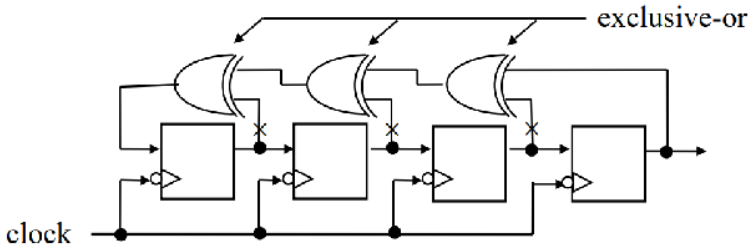

Figure 2 Feedback Shift Register State Machine

The modulator uses an AND gate to modulate the message signal with the carrier frequency at 40 KHz. It does it by outputting a “1” whenever the message is a “1” and the carrier frequency is “1”, otherwise if the message is a “0” or the carrier frequency is a “0” then the output is a “0”. This makes it so that now the transmitted signal is at the carrier frequency while retaining the original message.

The infrared LED uses a BJT as an amplifier from the AND gate. When a “1” is input to the BJT then the transistor turns on and supplies current to the LED which emits infrared light. If a “0” is output from the AND gate then the transistor turns off, so that no current will go through the LED. Then the LED will not emit an infrared signal making it a “0”.

The receiver is a phototransistor that receives infrared light and converts that into a current. This can be modeled by a BJT whose base the receiver of infrared light and the collector and emitter are regular NPN terminals. This phototransistor is then fed into the trans-impedance amplifier.

The trans-impedance amplifier converts a current into a voltage by Vout = Iin * R, where R is the resistance between the output of the op-amp and the non-inverting pin.

The bandpass filter then filters the signal with a center frequency of Figure 3 and a mid band gain of 2. The bandpass filter attempts to filter the noise from the environment so that the only signal that is being received is the carrier frequency. We used a two op-amp bandpass filter with a TL072 as the integrated circuit.

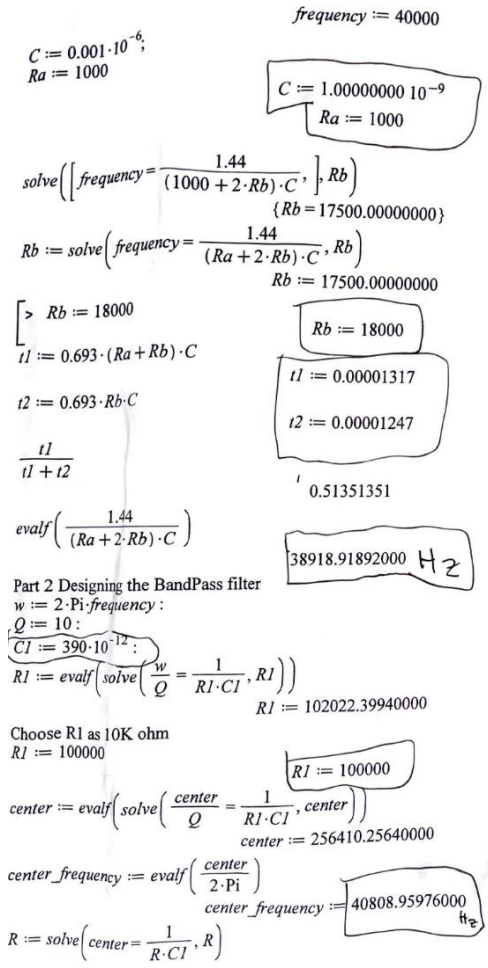

Figure 3 Calculation of the bandpass parameters

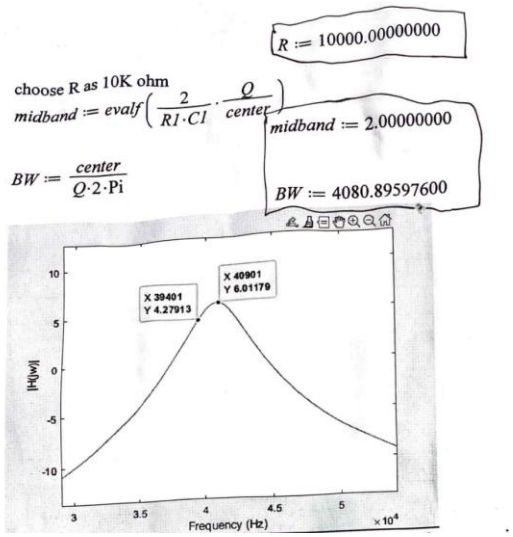

Figure 4 Matlab plot of calculated bandpass

The envelope detector is designed to demodulate the signal so that the message signal can be read. It uses an op-amp and diodes to half-wave rectify the signal and then capacitors smooth out the waveform creating an average from the modulated signal. The capacitors also cannot load the op-amp because it cannot supply much current. The other threshold of the envelope is the averaged value of the signal over a long period of time creating a moving threshold that will self-adjust.

The next stage of the receiver is the comparator, and its purpose is to set a threshold; once that threshold is reached it will output a "1". The inputs to the comparator are the envelope and the threshold from the envelope detector. The envelope is the average of the message, and the threshold is the envelope averaged even longer giving a self-adjusting threshold.

The timing recovery system creates the bit rate of the PSG so that the flip-flop has an accurate clock. The timing recovery system works by detecting the edge of the output of the comparator. It will then wait until 10 clock cycles have passed to output a "1" and then wait for another 10 cycles before it will register a new edge. The output will be a reconstructed bit clock from the

transmitter bit clock. This clock is then fed into the last stage, D flip-flop. The purpose of the D flip-flop is to create an output that has the same frequency as the bit clock. Its inputs are the comparator output and the timing recovery system output. The flip-flop will only change its output every clock cycle and it will follow the comparator. If the comparator is a “1” then the output will become a “1” at the next clock cycle and it will do the same thing if a “0” is the input.

The relationship between each subsystem is closely entailed in the System block diagram found in Figure 5.

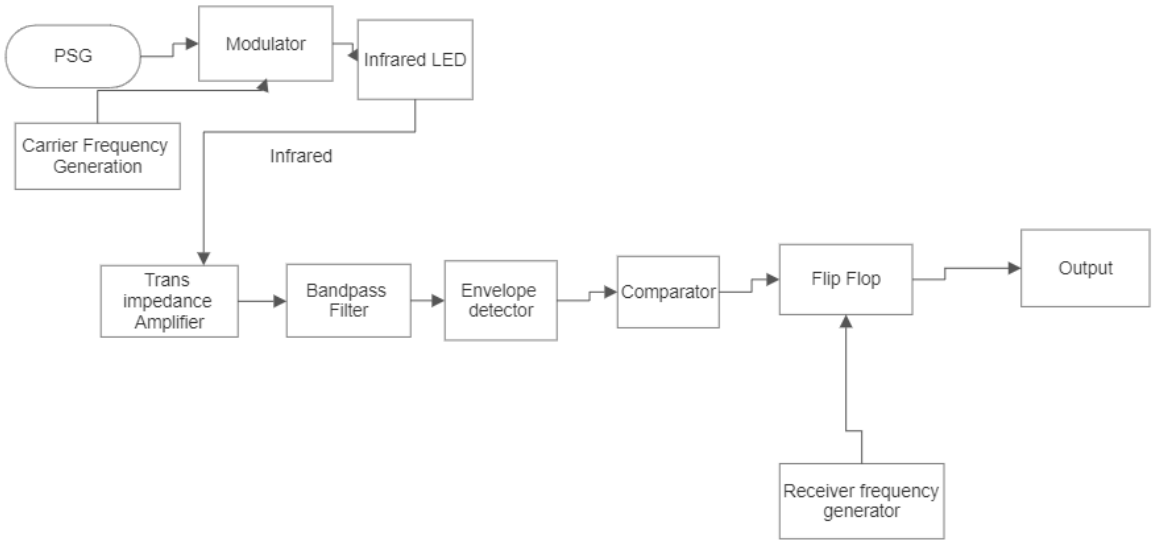

Figure 5 System block diagram

Circuit Documentation

The transmitter circuit subsystem diagrams can be found in Figures 6 to 9 with their respective inputs and outputs. The receiver circuit diagrams can be found in Figures 10 to 15 alongside their respective inputs and outputs.

Transmitter Subsystems

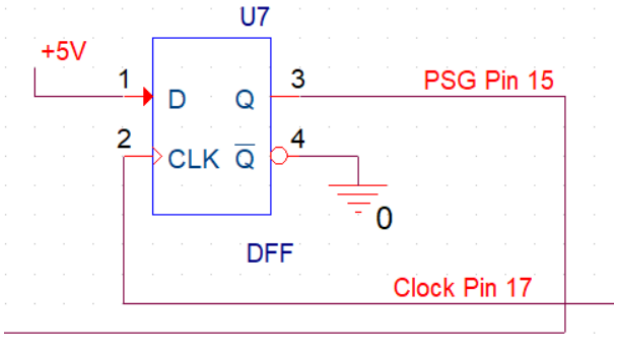

Figure 6 Pseudorandom Signal Generator

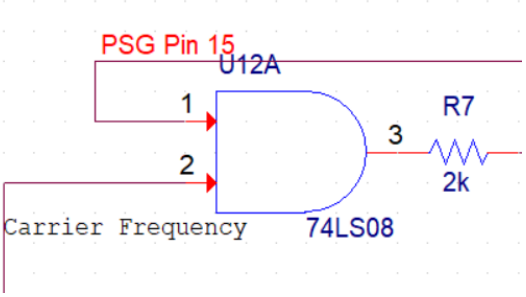

Figure 7 AND Gate Modulator

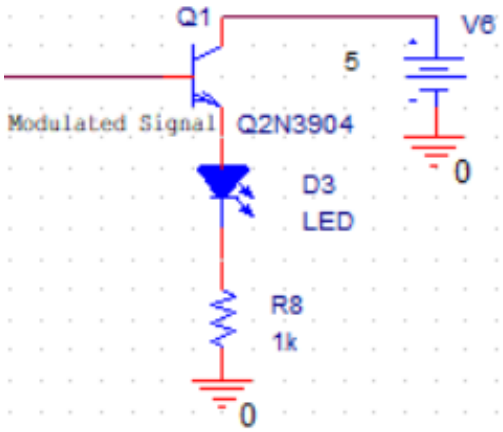

Figure 8 Infrared LED and BJT

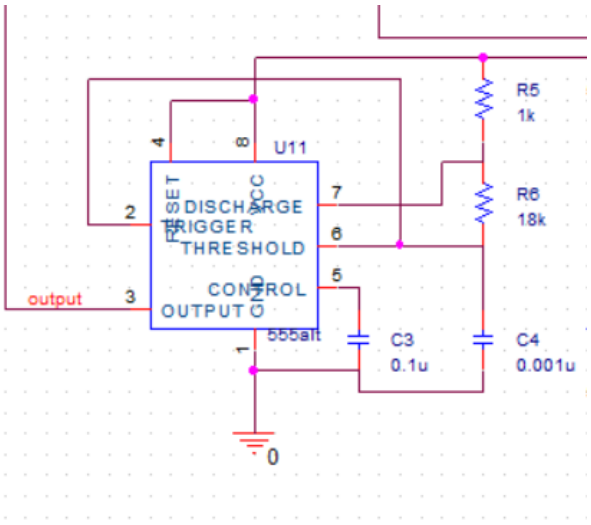

Figure 9 Carrier Frequency

Receiver Subsystems

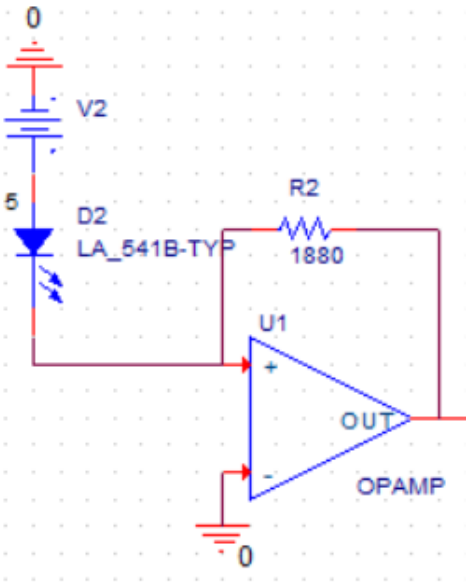

Figure 10 Transimpedance Amplifier

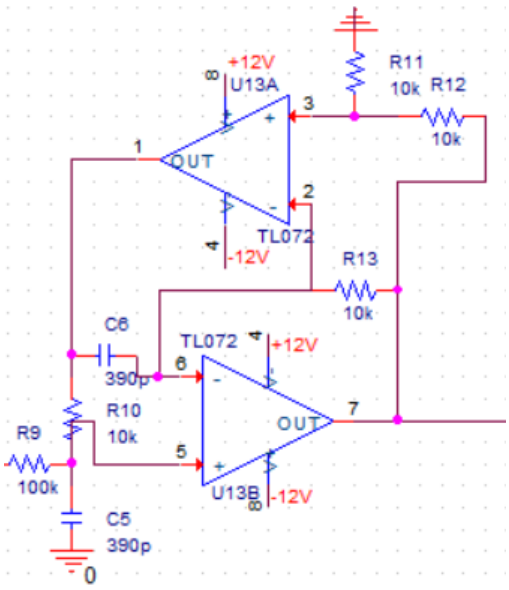

Figure 11 Band-Pass Filter

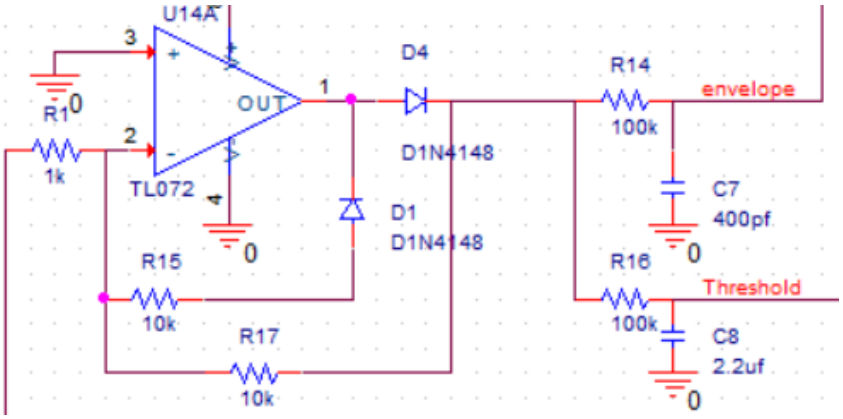

Figure 12 Envelope Detect

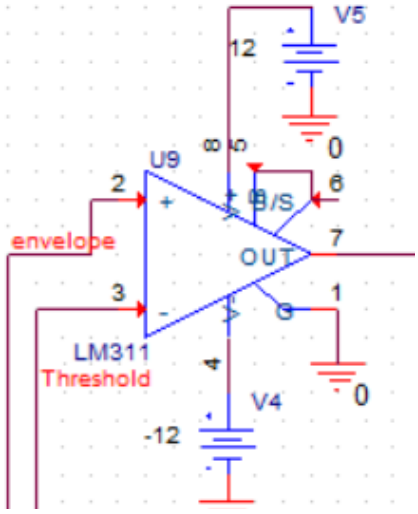

Figure 13 Comparator

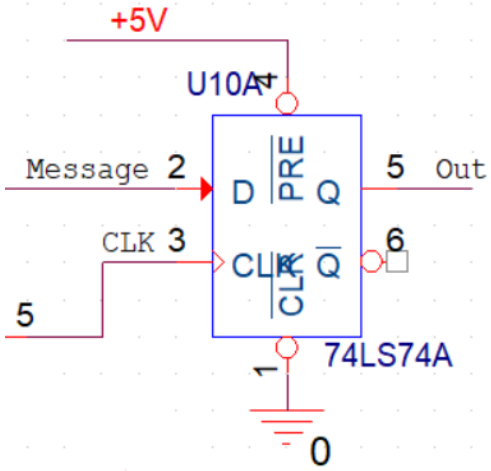

Figure 14 Output Flip Flop

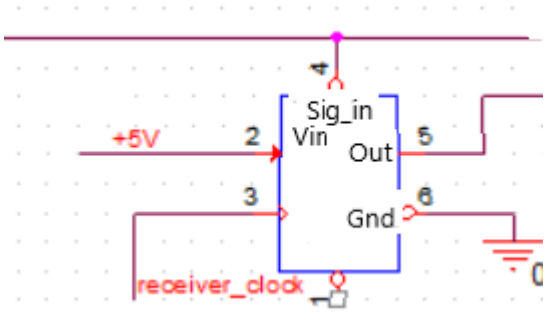

Figure 15 Timing Recovery System

The timing recovery system's state diagram can be found in the figure below, where all 20 state operations are entailed. The 4-bit PSG operation can be found in Figure 17

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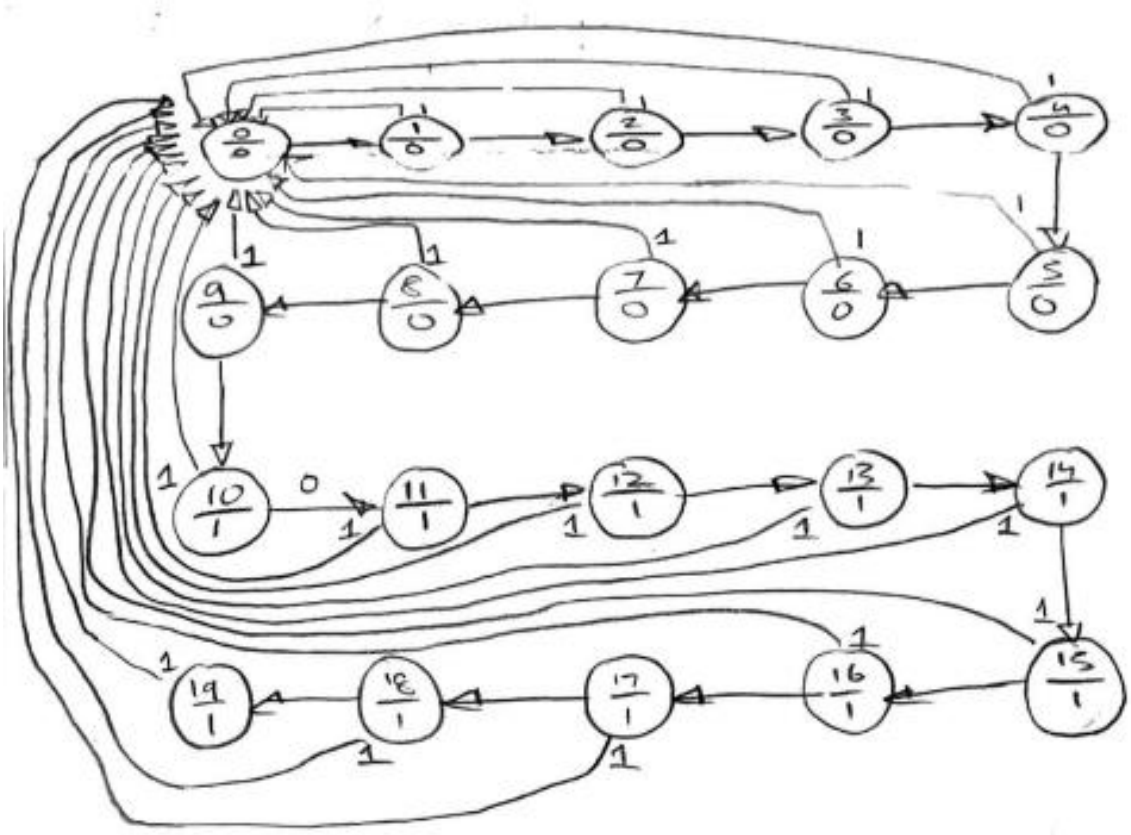


Figure 16 State diagram for timing recovery system

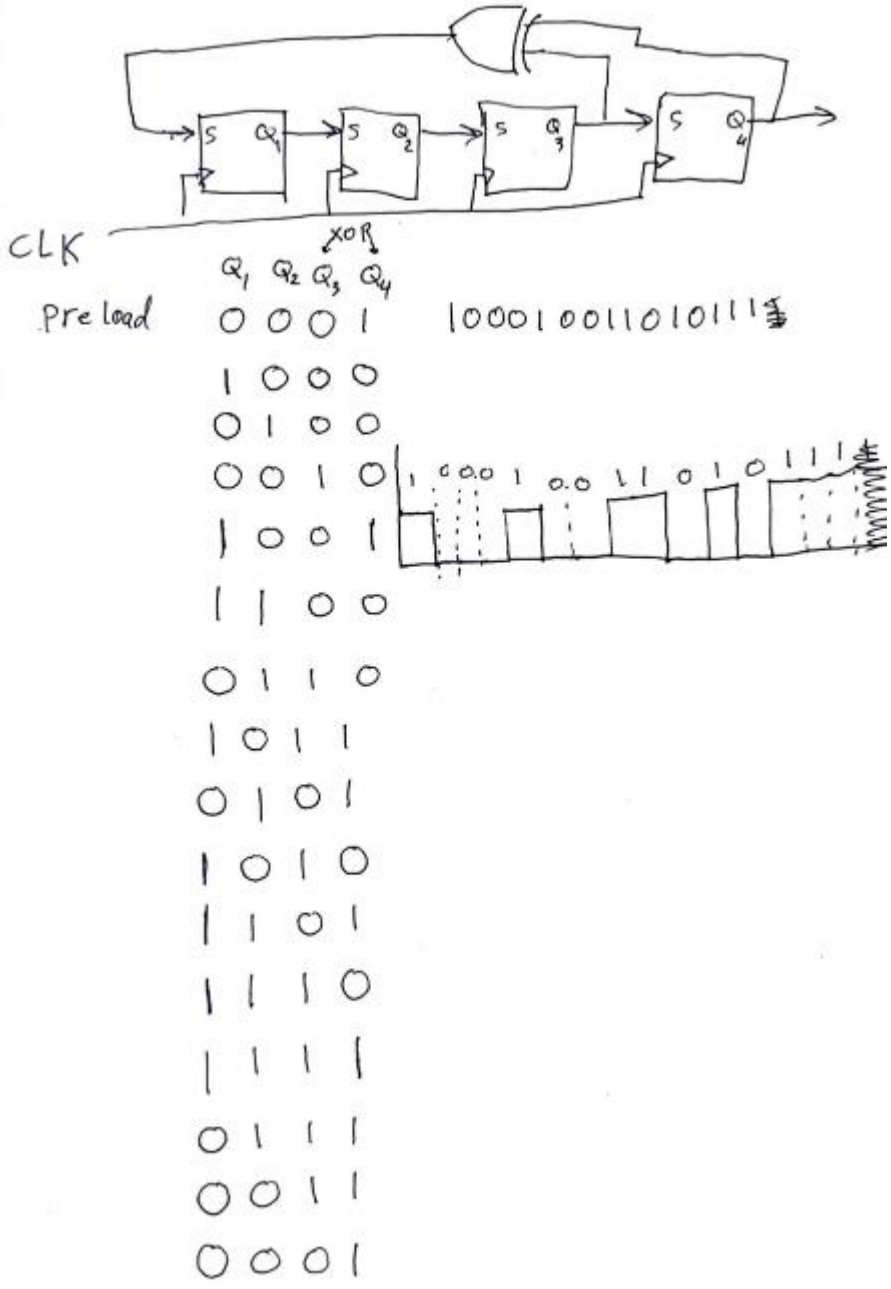


Figure 717 4-bit PSG internal operation

Measurements

Transmitter Validation

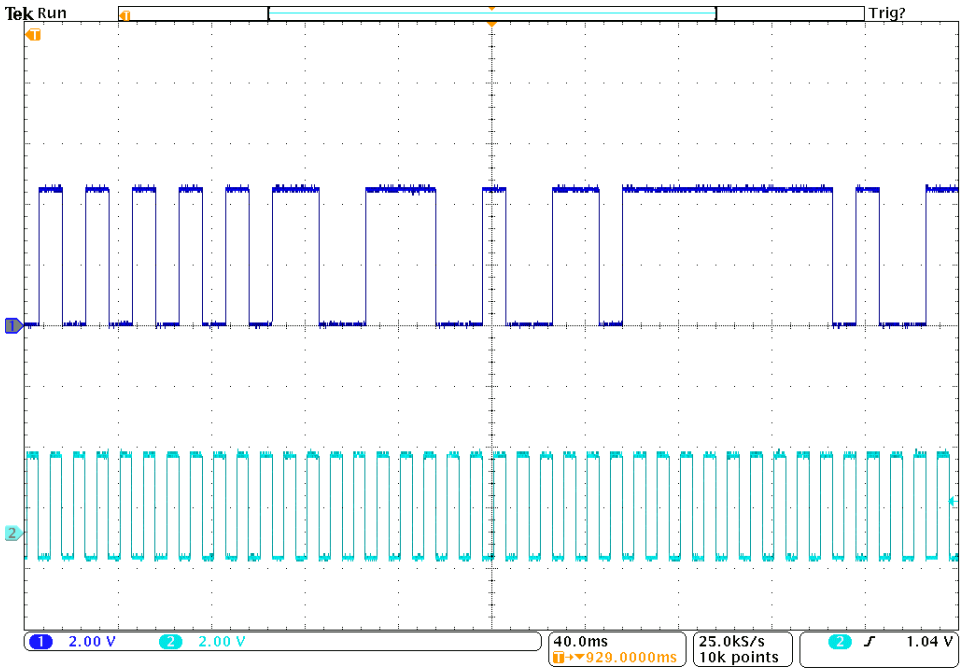


Figure 18 Output of the PSG

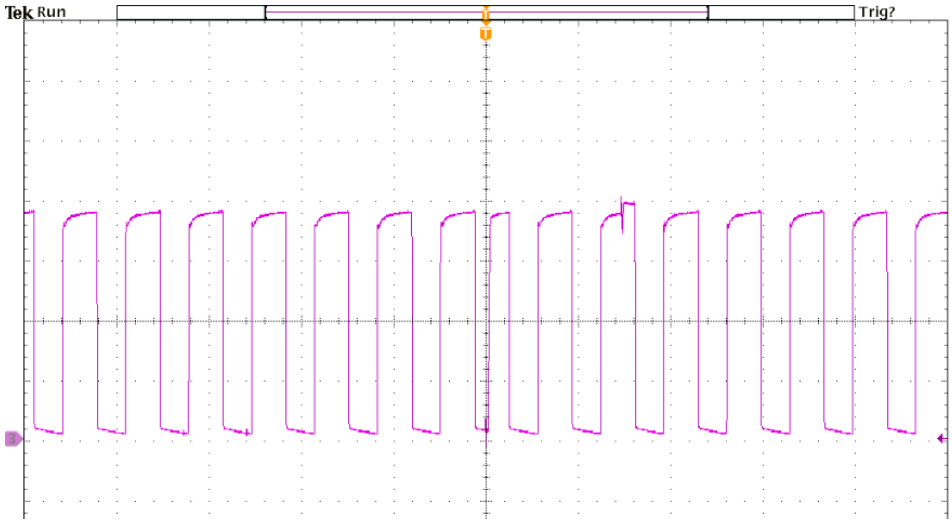


Figure 19 Output of the Oscillator prior to fine-tuning

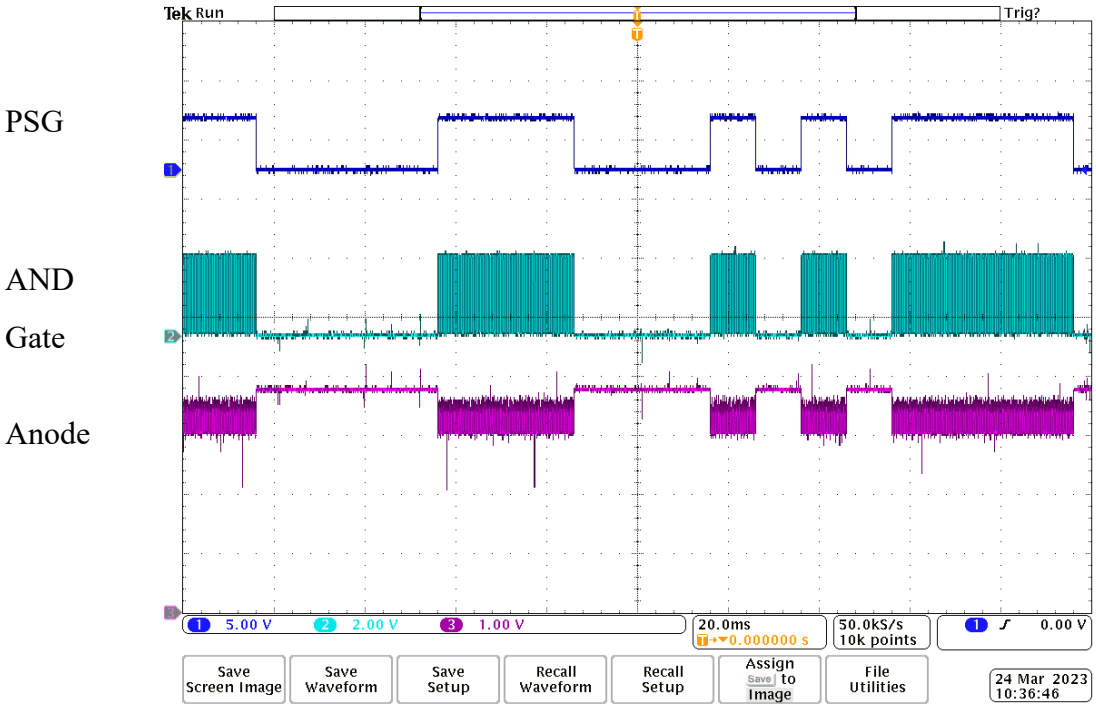


Figure 20 Output of the PSG, AND gate and LED anode

The PSG can be validated by Figure 18 which proves that a pseudo-random message can be generated over multiple clock cycles. The output of the oscillator can be verified in Figure 19 where the frequency of the oscillator was measured to be 36kHz. The last stage of the transmitter can be verified in Figure 20, where the output of the PSG, AND gate, and the anode of the LED can be viewed. The modulator subsystem is working correctly as whenever the PSG output is high, the AND gate produces a 1 and whenever the output of the PSG is low, the output of the AND gate is a 0.

Receiver Validation

PSG

Trans-

Impedance

Amplifier

BPF

Bit clock

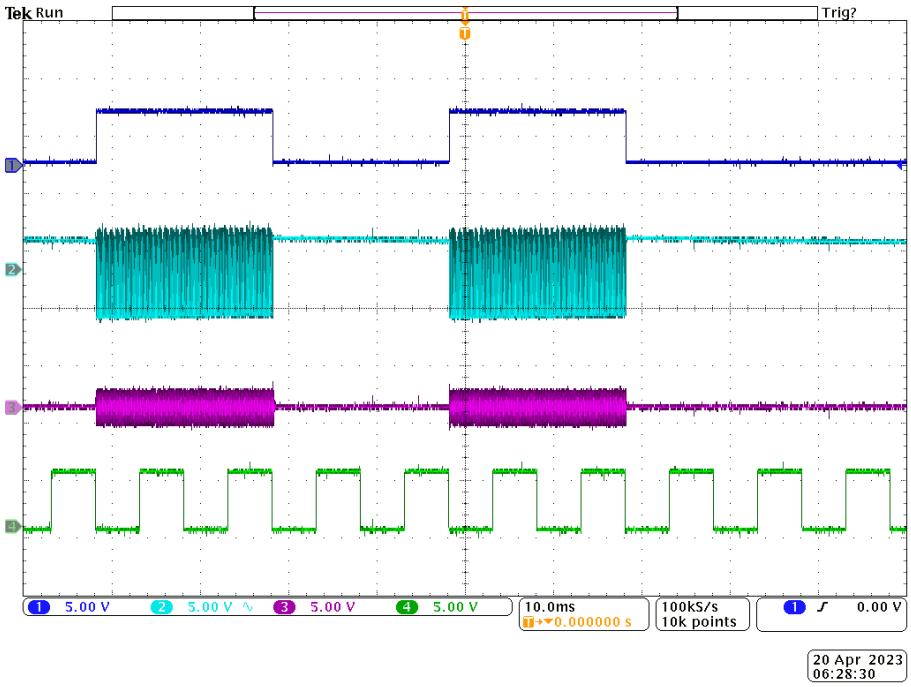


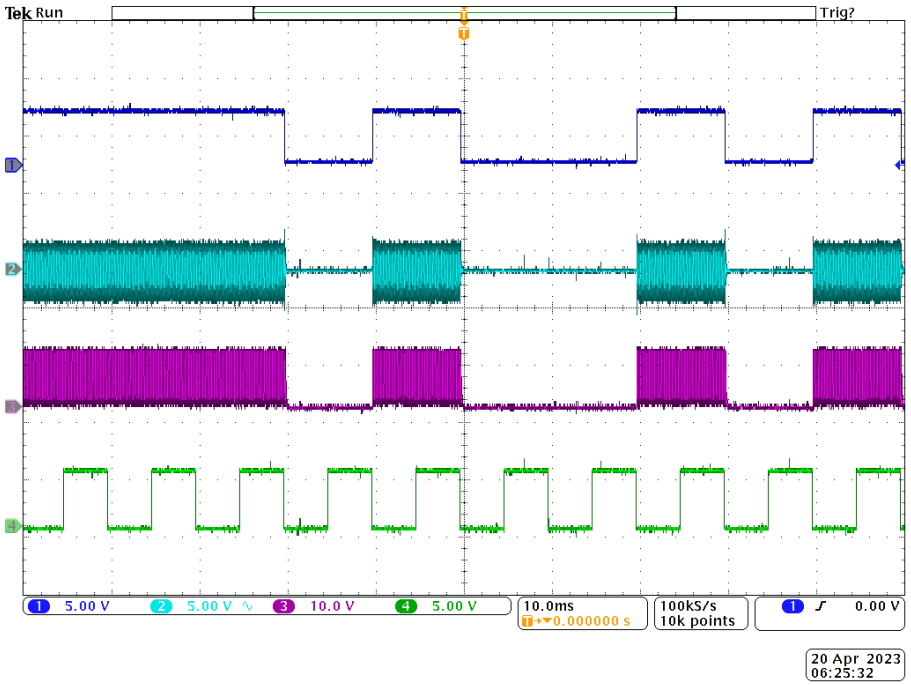
Figure 21 Output of the PSG, transimpedance amplifier, bandpass filter and bit clock

PSG

BPF

Envelope

Bit clock



PSG

Comparator

D flip flop

Bit clock

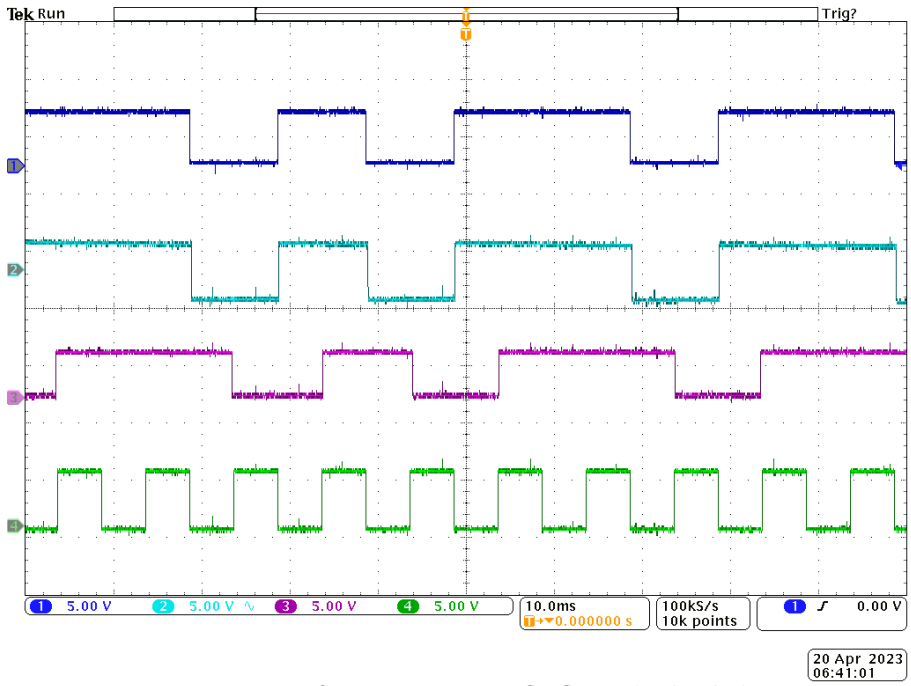


Figure 23 Output of PSG, comparator, D flip flop and Tx bit clock

PSG

D Flip flop

Tx Bit clk

Rx Bit clk

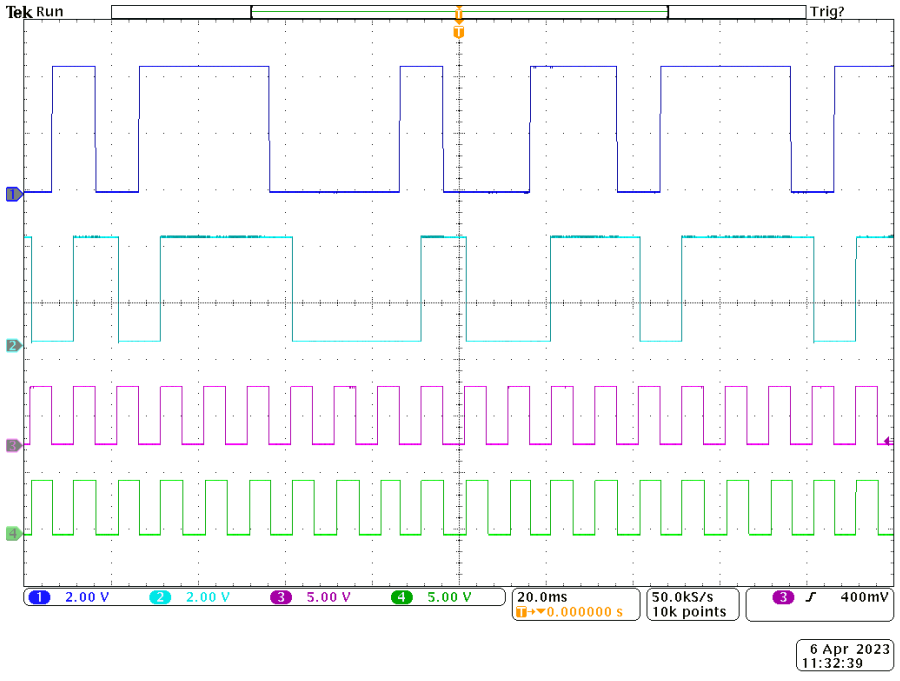


Figure 24 Output of PSG, D flip flop, TX bit clock, and Rx bit clock

The receiver first picks up a signal through the phototransistor that then passes through the trans-impedance amplifier which can be verified on channel 2 of Figure 21 which looks like an

amplified version of the anode signal on channel 4 of Figure 20 on the transmitter verification section. The output of the trans-impedance amplifier then flows into the bandpass filter. The output of the bandpass filter can be seen in Figure 22, which eliminates noise in the signal allowing for the transmitted signal at 40kHz to be isolated. The output of the envelope can also be verified by Figure 22, where the envelope is seen to demodulate the signal which feeds into the comparator. The output of the comparator can be verified in Figure 23, where the signal is a uniform '1' when the output of the PSG is high and a '0' when the output of the PSG is off. This output then feeds into the d flip flop which is supplemented by a timing recovery system that can be verified in Figure 24. The D flip flop exhibits a delay as it latches on the rising edge of the bit clock.

Discussion

The communication system project was able to be successfully set up and function at an operating distance of 27 inches. This is evidenced by the input-output relationship of the PSG signal and the D flip flop in Figure 24. During part of our communication system build, we had not noticed we had wired the trans-impedance amplifier incorrectly, which was significantly decreasing the gain of the system as well as the transmission length. We were able to fix the issue, jumping from a transmission length of 12 inches to over double our initial results. We also had to adjust the resistor values of the oscillator to modulate the PSG signal at 40kHz. Similarly, we finetuned the bandpass filter as well to adjust the center frequency at which the signal could be recovered and demodulated. During the lab, we managed to fry our pic by reversing the connections, so it is highly recommended to label the pins on the Pspice schematic and to continuously refer to the datasheet for the given part. The recovered data above a transmission length of 27 inches introduced a variety of errors to the system. For future students, it is

necessary to continuously troubleshoot the lab should an error arise and to document all wiring throughout the labs.

Instructor verification of System Operation

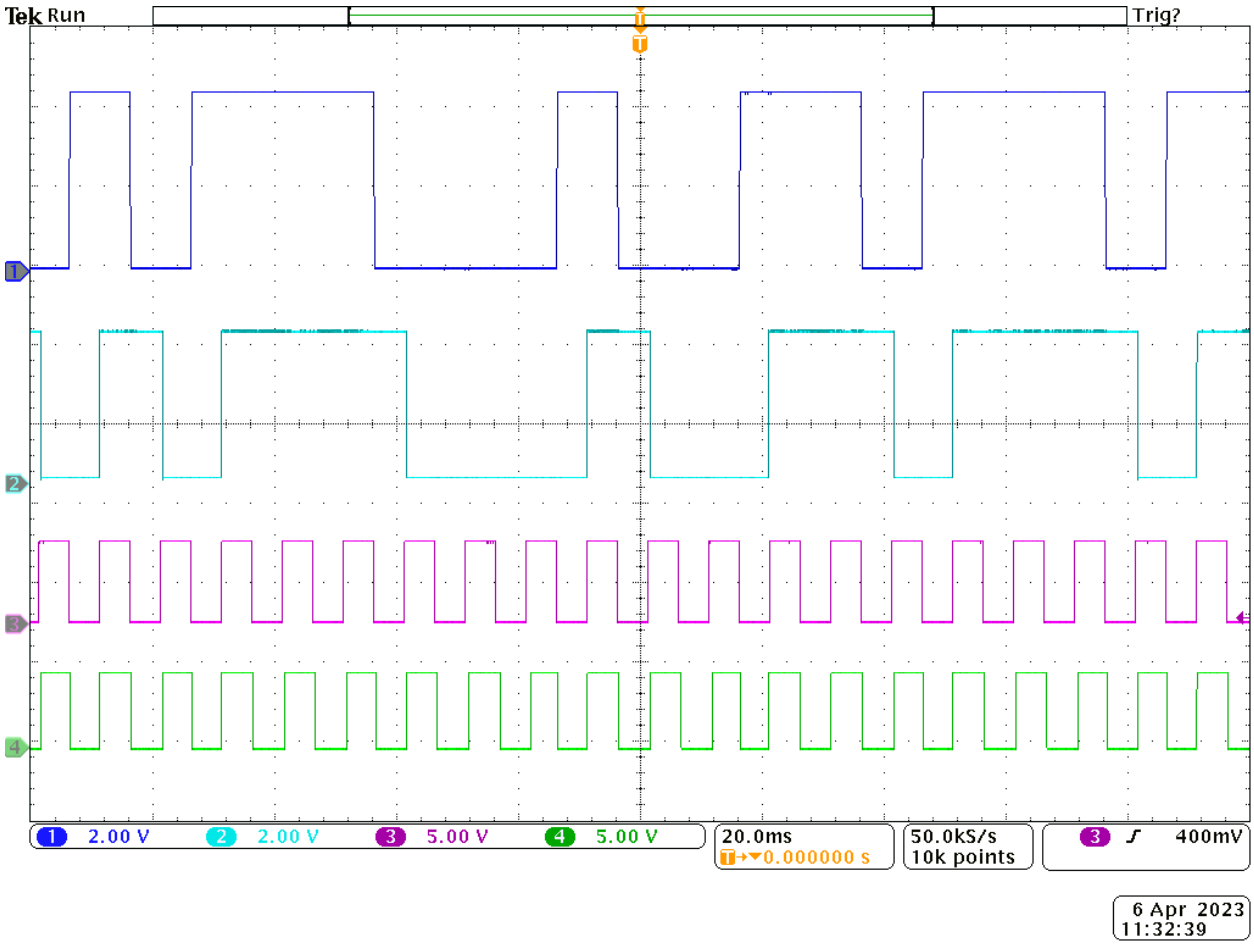


Figure 25 Oscilloscope capture of the final system

Mark A. Yoder may